WHAT IS CLAIMED IS:

1. An improved method for providing a processor access to image data, said processor having a memory space of a given size, the method comprising:

receiving an image for processing;

creating first, second, and third swappable windows for accessing image data from said image, said windows being swappable so that any two are available within the memory space of the processor while a third is being loaded in a background memory;

after initializing two of the windows with image data from said image and affixing those windows in the memory space of the processor as left and right adjacent windows, providing access to image data by performing substeps of:

i. loading the window that is not affixed in the memory space of the processor with image data from said image, said window temporarily comprising a shadow window that is loaded in the background memory,

ii. swapping said windows such that the left window is removed from the memory space of the processor, the right window now becomes the left window in the memory space of the processor, the shadow window now becomes the right window in the memory space of the processor, and the left window removed from the memory space of the processor now becomes a temporary shadow window to be loaded in the background memory, and

iii. providing access to the then-current left and right windows in the memory space of the processor for supporting image processing of said image.

2. The method of claim 1, repeating substeps i - iii until the entire image has been processed.

3. The method of claim 1, wherein said image comprises a megapixel image.

4. The method of claim 1, wherein said processor comprises a digital signal processor (DSP) having a small address space relative to the image.

5. The method of claim 1, wherein each said window comprises an 8x8 pixel window.

6. The method of claim 1, wherein any two windows present in the address space of the processor are organized as a 16x8 pixel block.

7. The method of claim 1, wherein the background memory comprises a DRAM.

8. The method of claim 1, wherein the background memory has an address space that is not directly accessible to the processor.

9. The method of claim 1, wherein the image has a size that is too large for the processor to access directly.

10. The method of claim 1, wherein the image has a size that is not too large for the processor to access directly.

11. The method of claim 1, wherein each of the values within each window is at a fixed memory address location relative to the window, as the window slides across the image.

12. The method of claim 1, wherein the image is processed by vertically sliding the windows across the image.

13. The method of claim 1, wherein the image is processed by horizontally sliding the windows across the image.

14. The method of claim 1, wherein the image is processed by both vertically and horizontally sliding the windows across the image.

15. The method of claim 1, wherein each said window comprises a pixel window having a bit width appropriate for a digital imaging processing application of interest.

16. The method of claim 15, wherein the digital imaging processing application of interest includes digital filtering of an image of a given size.

17. The method of claim 1, further comprising:

providing additional windows, so that the method may affix additional windows in the memory space of the processor at a given point in time.

18. The method of claim 1, further comprising:

providing additional windows, so that the method may background load additional windows in the memory space of the processor at a given point in time.

19. An apparatus for facilitating digital image processing, the apparatus comprising:

multiple two-dimensional image storage elements, including active and background ones;

a first control mechanism to temporarily map some of the two-dimensional image storage elements into an address space of a processor, whereupon those two-dimensional image storage elements become active in the address space of the processor;

a mechanism to background load one of the two-dimensional image storage elements that is not currently active in the address space of the processor; and

a second control mechanism to swap in the two-dimensional image storage element that has been background loaded into the address space of the processor, whereupon that two-dimensional image storage element becomes active in the address space of the processor.

20. The apparatus of claim 19, wherein, upon activation of said second control mechanism, one of the active two-dimensional image storage elements is no longer active in the address space of the processor.

21. The apparatus of claim 19, wherein said mechanism to background load includes a DMA engine.

22. The apparatus of claim 21, wherein said DMA engine issues an interrupt to signal the processor when background loading has completed.

23. The apparatus of claim 19, wherein said processor comprises a digital signal processor (DSP).

24. The apparatus of claim 19, wherein said two-dimensional image storage elements comprise at least two active windows that are active in the address space of the processor and at least one shadow window that is not active in the address space of the processor.

25. The apparatus of claim 24, wherein said at least two active windows comprise left and right active windows.

26. The apparatus of claim 25, wherein after a shadow window is loaded with appropriate image data and brought into the address space of the processor, the then-current right active window now becomes a new left active window, the prior left window now becomes a new shadow window, and the just-loaded shadow window now becomes a new right active window.